

Description

[METHOD OF FORMING LDD OF SEMICONDUCTOR DEVICES]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92113180, filed on May 15, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a method of making a lightly doped drain (LDD) of a semiconductor device. More particularly, the present invention relates to a method of making an LDD of a low temperature polysilicon thin film transistor (TFT) and a method of making an LDD of a metal oxide semiconductor (MOS) transistor.

[0004] Description of the Related Art

[0005] Distinguishable from conventional amorphous silicon TFT, low temperature polysilicon TFT can have electron mobility of above $200 \text{ cm}^2/\text{V}\cdot\text{sec}$. Consequently, TFT devices

can be made in smaller size and with higher aperture ratio so as to enhance the lightness of display panels and decrease power consumption. In addition, part of driving circuits, due to the enhanced electron mobility, the TFT can be formed simultaneously on the glass substrate, so as to improve the property and reliability of the liquid crystal display (LCD) panel and to significantly lower the fabrication costs of the LCD panel. Therefore, the manufacture costs of low temperature polysilicon TFT panels are much lower than the amorphous silicon TFT panels. Moreover, low temperature polysilicon TFT panels, which are characteristically thin in thickness, light in weight and superior in resolution, are especially suitable for making light, portable and power-saving mobile terminal products.

[0006] Earlier processes of making low polysilicon TFT panels include using semiconductor apparatus via solid phase crystallization (SPC). Since such processes are performed at a high temperature up to 1000 °C, quartz substrates with high melting points must be used. Due to higher costs of quartz substrates compared to glass substrates and size restrictions, panels with quartz substrates can be made in sizes of 2 to 3 inches, and thus only small panels

were developed in the past. More recently, with the development of laser technologies, a method of laser crystallization or excimer laser annealing is utilized to transform an amorphous silicon layer to a polysilicon layer. In the process of laser scanning, amorphous silicon is recrystallized to form polysilicon at a temperature lower than 600 °C. Thus, glass substrates can be used for making larger TFT LCD panels.

[0007] Figs. 1A to 1D are cross-sectional views illustrating steps of a process of forming an LDD of a conventional low temperature polysilicon TFT.

[0008] Referring to Fig. 1A, a patterned polysilicon layer 102 is formed on a substrate 100. In the process of forming the polysilicon layer 102, an amorphous silicon layer (not shown), deposited on the substrate 100, is first transformed to a polysilicon thin film via laser annealing and then defined via a photolithography process and an etching process to form the polysilicon layer 102.

[0009] Referring to Fig. 1B, a patterned photoresist layer 104 is formed on the substrate 100, wherein the photoresist layer 104 exposes a area predefined for forming source/drain. Subsequently, an ion implantation process 106 is performed by using the photoresist layer 104 as a mask

so as to implant ions into the polysilicon layer 102 not covered by the photoresist layer 104 to form a source 102a and a drain 102b.

[0010] Referring to Fig. 1C, after the photoresist layer 104 is removed, an insulating layer 108 is formed on the substrate 100 to cover the source/drain 102a/102b. A gate 110 is then formed on the insulating layer 108.

[0011] Referring to Fig. 1D, a patterned photoresist layer 112 is formed on the insulating layer 108, exposing the gate 110 and a region predefined to form an LDD. An ion implantation process 114 is then performed by using the photoresist layer 112 and the gate 110 as a mask to implant ions into the portion not covered by the photoresist layer 112 and the gate 110 to form an LDD 103. The portion located between the source/drain 102a/102b and the LDD 103 is a channel region 102c of the device.

[0012] Therefore, the conventional method of making an LDD of a low temperature polysilicon TFT requires two masking steps and two ion implantation steps, and the process is rather complicated. Especially, since it is not easy to control mask position in two masking steps and may get misaligned, accordingly, it is rather difficult to precisely control the width of the LDD. Any deviation in mask position

between two mask steps will lead to discontinuity of the source/drain and the LDD at the interface between the source/drain and the LDD, which will adversely affect the electrical properties of the device.

SUMMARY OF INVENTION

- [0013] Accordingly, in the light of the foregoing, one object of the present invention is to provide a method of forming an LDD of a semiconductor device with a view to simplify the complicated conventional method that requires two masking steps and two ion implantation steps for forming an LDD of low temperature polysilicon TFT.
- [0014] Another object of the present invention is also to provide a method of forming an LDD of a semiconductor device to resolve the problems resulting from mask mis-alignment between the two masking steps.
- [0015] Another object of the present invention is to provide a method of forming an LDD of a semiconductor device, in which both the source/drain and the LDD can be formed by performing a single masking step and a single ion implantation step.
- [0016] In accordance with the above objects and other advantages, as embodied and broadly described herein, the present invention provides a method of forming an LDD of

low temperature polysilicon TFT and a method of forming an LDD of MOS transistor. A substrate having a polysilicon layer thereon is provided. The polysilicon layer comprises a first region and a second region. Preferably, the method of forming the polysilicon layer include depositing an amorphous silicon layer on the substrate, transforming the amorphous silicon layer into a polysilicon layer via laser annealing, and further defining the polysilicon layer via photolithographic and etching processes. After forming the polysilicon layer, a photoresist layer is formed on the polysilicon layer. A mask having a non-exposing region, an exposing region and a partial-exposing region is set above the photoresist layer. In the present invention, the partial-exposing region of the mask comprises a pattern of a plurality of long strips. A photolithographic process is then performed to pattern the photoresist layer for exposing the first region and covering the second region of the polysilicon layer. The photoresist layer covering the second region comprises a middle portion and an edge portion, wherein the middle portion is thicker than the edge portion. The middle portion and the edge portion of the photoresist layer are formed in different thickness through the non-exposing region and the partial-ex-

posing region. Then, an implantation process is performed by using the patterned photoresist layer as a mask for forming a source/drain in the first region of the polysilicon layer and, at the same time, forming an LDD in the polysilicon layer covered by the edge portion of the photoresist layer.

[0017] In the method of forming an LDD of a semiconductor device, a substrate having a first region and a second region thereon is provided. A photoresist layer is then formed on the substrate. A mask is set above the photoresist layer. The mask comprises a non-exposing region, an exposing region and a partial-exposing region. In the present invention, the partial-exposing region of the mask comprises a pattern of a plurality of long strips. A photolithographic process is then performed to pattern the photoresist layer for exposing the first region of the polysilicon layer and covering the second region of the polysilicon layer. The photoresist layer covering the second region comprises a middle portion and an edge portion, wherein the middle portion is thicker than the edge portion. The middle portion and the edge portion of the photoresist layer are formed in different thickness through the non-exposing region and the partial-exposing region of the

mask, respectively. Then, an implantation process is performed by using the patterned photoresist layer as a mask for forming a source/drain in the first region of the substrate and, at the same time, forming an LDD in the substrate covered by the edge portion of the photoresist layer.

[0018] The method of the present invention is much simple comparing to the prior art since both the source/drain and the LDD of the device are formed in a single ion implantation step in the present invention.

[0019] According to one aspect of the present invention, the source/drain and the LDD of the device are simultaneously formed by performing a single masking step and a single ion implantation step, and therefore the problems resulting from mask mis-alignment between the two masking steps as described in the conventional method can be effectively avoided.

[0020] According to another aspect of the present invention, the pattern design of the partial-exposing region of the mask can be utilized to control the thickness of the patterned photoresist layer. Further, the post-exposure baking temperature can be utilized to control the density of the photoresist layer to further control the ion doping concentra-

tion in the LDD.

[0021] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0022] The accompanying drawings are comprised to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0023] Figs. 1A to 1D are cross-sectional views illustrating steps in the process of making an LDD of a low temperature polysilicon TFT according to prior art.

[0024] Figs 2A to 2D are cross-sectional views illustrating steps in a process of making an LDD of a low temperature polysilicon TFT according to a preferred embodiment of the invention.

[0025] Fig. 3 shows a top view of the mask in Fig. 2C.

[0026] Figs. 4A to 4D are cross-sectional views illustrating steps in a process of making a semiconductor device according

to a preferred embodiment of the invention.

DETAILED DESCRIPTION

- [0027] Referring to Fig. 2A, a substrate 200 having a polysilicon layer 202 thereon is provided. The polysilicon layer 202 comprises a first region 201a and a second region 201b. In the preferred embodiment of the present invention, a method of forming the polysilicon layer 202 includes depositing an amorphous silicon layer (not shown) on the substrate 200, transforming the amorphous silicon layer into a polysilicon layer via laser annealing, and further defining the polysilicon layer 202 via photolithographic and etching processes.
- [0028] Referring to Figs. 2B and 2C, after the polysilicon layer 202 is formed, a photoresist layer 204 is formed on the polysilicon layer 202. A mask 206 is set above the photoresist layer 204, wherein the mask 206 comprises a non-exposing region 206a, an exposing region 206c, and a partial-exposing region 206b.
- [0029] In the preferred embodiment of the present invention, as shown in Fig. 3, the partial-exposing region 206b of the mask 206 comprises a pattern of a plurality of long strips. The partial-exposing region 206b of the mask 206 corresponds to a region predefined for forming an LDD. In the

partial-exposing region 206b, the width of the patterned long strips is, for example, 0.05 to 0.5 μm , and the distance between two adjacent patterned long strips is, for example, 0.05 to 0.5 μm . The non-exposing region 206a of the mask 206 corresponds to a region predefined for forming a channel region. The exposing region 206c corresponds to a region predefined for forming a source/drain.

[0030] Referring to Fig. 2C, photolithography and etching processes are performed to pattern the photoresist layer 204 to form a patterned photoresist layer 205 such that regions 201a and 201c of the polysilicon layer 202 are exposed and a region 201b of the polysilicon layer 202 remain covered by the patterned photoresist layer 205. The portion of the patterned photoresist layer 205 covering the second region 201b comprises a middle portion 205a and an edge portion 205b, wherein the middle portion 205a is thicker than the edge portion 205b. The middle portion 205a and the edge portion 205b of the photoresist layer 205 are formed in different thickness through the non-exposing region 206a and the partial-exposing region 206b of the mask 206. The thickness of the middle portion 205a of the photoresist layer 205 is, for example,

1 to 5 μm , whereas the thickness of the edge portion 205b of the photoresist layer 205 is, for example, 0.1 to 1 μm .

[0031] Referring to Fig. 2D, an implantation process 208 is performed using the photoresist layer 205 as a mask for forming a source 202a and a drain 202b in the regions 201a and 201c of the polysilicon layer 202 respectively, and at the same time, an LDD 203 is formed in the polysilicon layer 202 underneath the edge portion 205b of the photoresist layer 205. The portion of the polysilicon layer between the source/drain 202a/202b and the LDD 203 is a channel region 202c of the device. In the embodiment, the ion concentration in the source/drain 202a/202b is, for example, 1×10^{14} to 1×10^{15} ions/ cm^2 , the ion concentration in the LDD 203 is, for example, 1×10^{12} to 1×10^{14} ions/ cm^2 , and the width of the LDD 203 is, for example, 0.1 to 1 μm .

[0032] Subsequently, the photoresist layer 205 is removed, a gate structure including a gate insulating layer, a gate and source/drain metal lines, is formed over the channel region 203c for forming a low temperature polysilicon TFT.

[0033] In the method of the present invention of forming an LDD, a mask having a partial-exposing region is utilized to

form a patterned photoresist layer with various thickness, can be used to form a semiconductor device in a logical circuit, a detailed description of which is presented as follows.

[0034] Referring to Figs. 4A to 4D, a substrate 300 having a first region 301a and a second region 301b thereon is provided. A photoresist layer 302 is then formed on the substrate 300. A mask 306 is set above the photoresist layer 302. The mask 306 comprises a non-exposing region 306a, an exposing region 306c, and a partial-exposing region 306b. In the embodiment, the partial-exposing region 306b of the mask 306 comprises a pattern of a plurality of long strips. The width of each patterned long strip is, for example, 0.005 to 0.05 μm , and the distance between two adjacent patterned long strips is, for example, 0.005 to 0.05 μm .

[0035] Further, photolithography and etching processes are performed to pattern the photoresist layer 302 to form a patterned photoresist layer 305 such that a first region 301a of the substrate 300 is exposed, and a second region 301b of the substrate 300 remain covered by the patterned photoresist layer 305. The patterned photoresist layer 305 covering the second region 301b comprises a

middle portion 305a and an edge portion 305b, wherein the middle portion 305a is thicker than the edge portion 305b. In the preferred embodiment of the present invention, the thickness of the middle portion 305a of the photoresist layer 305 is, for example, 0.1 to 1 μm , and the thickness of the edge portion 305b of the photoresist layer 305 is, for example, 0.01 to 0.1 μm . It should be noted that the middle portion 305a and an edge portion 305b of the photoresist layer 305 are formed in different thickness through the non-exposing region 306a and the partial-exposing region 306b of the mask 206.

[0036] Referring to Fig. 4C, an implantation process 308 is performed using the photoresist layer 305 as a mask for forming a source 310a and a drain 310b in the first region 301a of the substrate 300, and at the same time, an LDD 312 is formed in the substrate 300 underneath the edge portion 305b of the patterned photoresist layer 305. In the preferred embodiment of the present invention, the ion concentration in the source/drain 302a/302b is, for example, 1×10^{13} to 1×10^{16} ions/ cm^2 , the ion concentration in the LDD 312 is, for example, 1×10^{12} to 1×10^{15} ions/ cm^2 , and the LDD 312 is formed in a width of, for example, 0.01 to 0.1 μm .

[0037] Referring to Fig. 4D, after the photoresist layer 305 is removed, a gate insulating layer 314 is formed on the substrate 300, and then a gate 316 is formed on the gate insulating layer 314 for forming an MOS semiconductor device.

[0038] In the method of forming an LDD of low temperature polysilicon TFT of the present invention, both the source/drain and the LDD of the device are formed by performing a single masking step and a single ion implantation step. Consequently, not only the process can be simplified but the difficulties of controlling mask position in order avoid mis-alignment between two masking steps of the prior art can also be effectively avoided. In addition, because both the source/drain and the LDD of the MOS device are formed by a single ion implantation step, and therefore the source/drain and the LDD are in continuity with each other, and thus the reliability of the device can be effectively promoted. Specifically, the method of the present invention utilizes the pattern of the partial-exposing region of the mask to control the thickness of the patterned photoresist layer and further to control the ion doping concentration in the LDD. Moreover, the post-exposure baking temperature is utilized to control the density of

the photoresist layer and also further to control the ion doping concentration in the LDD.

[0039] In view of the foregoing, the method of the present invention has the following advantages, for example: 1. The method of the present invention is much simple comparing to the prior art since both the source/drain and the LDD of the device are simultaneously formed in a single ion implantation step. 2. Because the source/drain and the LDD of the device are simultaneously formed in a single masking step and a single ion implantation step, and therefore the difficulties of controlling mask position in order to avoid mis-alignment of masks between two masking steps of the prior art can be effectively eliminated. 3. The partial-exposing region of the mask can be used to form a patterned photoresist layer having differential thickness so that the source/drain and the LDD can be formed in a single ion implantation step. Further, the thickness of the patterned photoresist layer can be controlled to control the doping concentration of the LDD. Furthermore, the post-exposure baking temperature may be varied to control the density of the patterned photoresist layer to further control the ion doping concentration of the LDD.

[0040] It will be apparent to those skilled in the art that various modifications and variations can be made to the features of the present invention without departing from the scope and spirit of the present invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.